IN THE SPECIFICATION

1. Amend the paragraph on page 6, starting at line 15 and ending at line 27, as follows:

The wireless device 10 includes a transmitter 4, a controller 6 which is a suitable microprocessor in the preferred embodiment, a receiver 8, and a counter 2 which is provided by a memory component and the microprocessor in the preferred embodiment. Device 10 may be a mobile unit, or any transceiver used in the industry. The transmitter 4 and receiver 8 establish connection with the wireless network (e.g. cellular network) in the manner well-known to persons skilled in the art, under control of the controller 6. Machine readable storage 9, comprising non-volatile memory, stores the duty cycle management system algorithm and information and parameters utilized thereby including ~~the parameters IC and DC~~ a first amount "IC" and a second amount "DC" representing the value of an increment count and the value of a decrement count, respectively, whereby the parameters IC and DC are fixed numbers for any given embodiment and used by the system in applying the duty cycle management method. In this embodiment a counter 2 is provided for use in controlling the active time of a transmitter.

2. Amend the paragraph bridging pages 7 and 8, namely lines 27-30 on page 7 and lines 1-16 on page 8 as follows:

Figures 2(a) and 2(b) are flowcharts showing the steps performed by the duty cycle management system which utilizes the controller 6, the counter 2 and memory 9. These flowcharts each represent a repetitive algorithm which is repeated for each time slot 13 and this algorithm is implemented in one or more computer programs which are executable by the controller 6 (microprocessor). Figure 2(a) shows the normal steps of the algorithm to be used for individual packet and burst packet transmission when a relatively high duty cycle limit is applied (e.g. 25%) and Figure 2(b) shows the special case steps of the algorithm to be used for individual packet and burst packet transmission when a relatively small duty cycle limit is applied (e.g. 2%). For a selected duty cycle of 25% in this illustrated example a firmware counter 2 increments by the increment count (IC) 15,16 amount of 4 upon each individual packet transmission 11 and decrements by the decrement count (DC) 17 amount of 1 upon each idle (receive) slot 12 (i.e. 1/4 equals 25%) whereas for a duty

cycle of 2% the counter 2 is incremented by 50 (i.e. IC=50) upon each individual packet transmission and decremented by 1 (i.e. DC=1) upon each idle (receive) slot (i.e. {fraction (1/50)} equals 2%). When the counter 2 exceeds a maximum counter amount equal to the predetermined number of timeslots per time window, being 1153 for these examples, the system halts any further transmissions because this means that, at this point in time, a ratio of 4 to 1 packets (representing a duty cycle of 25%) or 50 to 1 packets (representing a duty cycle of 2%) have been transmitted over the preceding window time period T.

3. Amend the paragraph bridging pages 8 and 9, namely lines 17-30 on page 8 and line 1 on page 9, as follows:

For the example of a 25% duty cycle limit a single packet burst of the maximum 23 packets will only increment the counter 2 by 92 counts (i.e. 4 x 23), which is far below the maximum count amount of 1153, so several bursts may be transmitted within one time window without pushing the counter amount close to the maximum count threshold 19. However, for the low duty cycle limit example of 2% a single packet burst can, if it consists of 23 packets, use up essentially all of the permissible time slots for a given time window. Consequently, as shown in Figure 2(b), for this special case example a packet burst may only be sent when the value of the counter 2 is zero. From a time line perspective this means that a 1.2 sec maximum-length burst transmission (i.e. 52 ms x 23=1.2 sec) leaves the counter 2 at its maximum value of 1150 for that increment level (IC) and this inhibits any further burst transmissions for the next period of 59.8 seconds calculated on the basis of 1150 x 52 ms. This represents the worst-case duty cycle limit of 2% and results in a calculated duty cycle value of 1.96% over the period of those 1150 timeslots which satisfies this duty cycle limitation of 2% (i.e. 1.2 sec divided by (59.8 sec+1.2 sec=1.2/61=1.96%).

4. Amend the paragraph on page 9 from line 2 to line 24, as follows:

As shown by Figure 2(a) ~~2~~, the special case algorithm of the duty cycle management system (i.e. the situation in which a single packet burst would render the counter close to the maximum counter amount within a single time window) is performed on an adaptive basis whereby one of two methods (algorithms), A or B, is selected and performed for the

transmission of bursts 22 and the selection of which algorithm is performed impacts upon the performance of the system in relation to the communications network. Figures 3(a) and 3(b) illustrate, graphically, the results of performing methods A and B, respectively, for a duty cycle (DC) limit of 2%. The steps of method A are performed when there have been no transmissions at all 20 (see Figure 3(a)) (i.e. no burst and no individual packet) for a number of timeslots equal to the predetermined number of timeslots per time window prior to the pending burst (i.e. the counter value 24 is zero and there must have been no increment to the counter during the immediately preceding time window). As shown by Figure 2(b), the counter is incremented 30 by IC for each packet in the burst. This limits the duty cycle of bursts plus individual packets to 2% over any double window period (2T) (i.e. any period of 2 minutes in this example). Application of this method will occur in networks where a burst is typically the first of a series of transmissions, and may be followed by a small number of individual packets such as an application-level acknowledgement packet (alternatively referred to herein as an `ACK` packet, being a type of packet used to acknowledge receipt of an incoming message). For purposes of network efficiency it is desirable to avoid delays in transmitting "ACK" packets as this may cause an unnecessary retransmission of the message and, thus, an "ACK" priority feature, as detailed more fully below, may be used in combination with duty cycle algorithm of the invention in order to enhance the overall network performance.

5. Amend the paragraph bridging pages 9 and 10, namely lines 25-30 on page 9 and lines 1-5 on page 10, as follows:

The steps of method B are performed when the value of the counter 24 is zero but the counter has been incremented 25 (see Figure 3(b)) during the immediately preceding window i.e where some individual packets have been sent during that window. For this method the counter is incremented 35 by 2 times the value of IC (i.e. by 100 in the foregoing example applying a 2% duty cycle limit) for each packet in a burst. Following the transmission of the burst in this example the value of the counter is 2300 (calculated on the basis of 100 times 23 packets) and this means that following a maximum-length burst all transmissions will be halted for one time window (i.e. 1 minute in this example) and any further burst will be halted for two time windows (i.e. 2 minutes in this example). Application

of this method will occur in networks where a burst typically ends a series of exchanges.

6. Amend the paragraph on page 10 from line 6 to line 17, as follows:

These two alternate burst-mode methods (A and B) are selected adaptively to yield best performance by using the following algorithm (this is also illustrated by Figure 2(a) ~~2~~):

IF

there have no transmissions during the preceding window

THEN

A: debit burst packets at 1 x IC each (IC=50 in the example) (It is necessary to exclude the reservation-request packet, or make the debit-rate decision at reservation-request time and not at burst transmit time or the above case will never be true.)

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B: debit burst packets at 2 x IC each (IC=50 in the example)